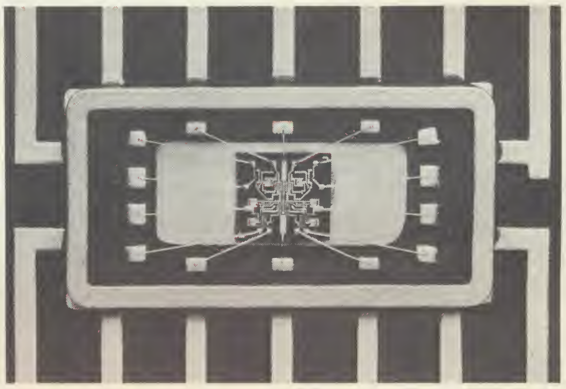
SERIES 54
BULLETIN NO. DL-S 657921, AUGUST 1965

HIGH-SPEED SATURATED DIGITAL CIRCUITS FOR GENERAL-PURPOSE SYSTEM APPLICATIONS

description

Series 54 integrated circuits have been designed and characterized for high-speed, general-purpose digital applications where high d-c noise margin and low power dissipation are important system considerations. Definitive specifications are provided for operating characteristics over the full military temperature range of –55°C to 125°C. This logic series includes the basic gating and flip-flop elements needed to perform practically all functions required of general-purpose digital systems.



TYPE SN5400 PRIOR TO CAPPING

features

LOW SYSTEM COST

- **maximum number of circuits per package through use of 14-lead package**

OPTIMUM CIRCUIT PERFORMANCE

- **high speed — typical propagation delay time 13 nsec**
- **high d-c noise margin — typically one volt**
- **low output impedance provides low a-c noise susceptibility**
- **waveform integrity over full range of loading and temperature conditions**
- **low power dissipation — 10 mw per gate at 50% duty cycle**
- **full fan-out of 10**

CONTENTS

†Patented by Texas Instruments Incorporated.

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS 22, TEXAS

design characteristics

Series 54 digital integrated circuits effect an optimization between saturated logic circuitry and monolithic semiconductor technology yielding high performance at lowest cost. In discrete component circuitry maximum use is made of lower cost components (diodes and resistors) instead of the higher priced transistors. However, in monolithic circuitry it costs no more to build transistors than diodes or resistors. Therefore, in Series 54, transistors are used to buffer the fluctuations in currents that occur as resistor values change. Also, the Series 54 multiple emitter transistor can easily be built in a monolithic bar to eliminate the need for conventional input diodes.

circuit operation

The transistor-transistor logic (TTL) used in Series 54 is analogous to diode-transistor logic (DTL) in certain respects. As shown in figure A, a low voltage at inputs A or B will allow current to flow through the diode associated with the low input, and no drive current will pass through diode D_3. If inputs A and B are raised to a high voltage, drive current will then pass through diode D_3.

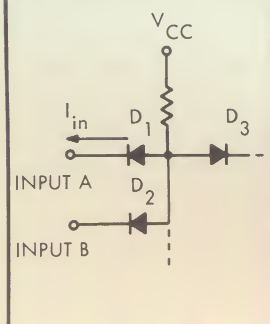


Figure A
Diode AND Logic

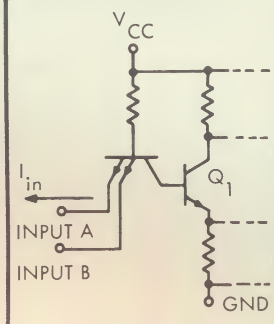


Figure B
Series 54 AND Logic

In Series 54 TTL circuitry, the multiple-emitter transistor performs the same function as the diodes in DTL (see figure B). However, the transistor action of the multiple-emitter transistor causes transistor Q_1 to turn-off more rapidly, thus providing an inherent switching-time advantage over the DTL circuit.

Although one-volt d-c noise margins are typical for Series 54 circuits, an absolute guarantee of 400 millivolts is assured for every unit. This is accomplished by testing each output and input as shown in figures C and D.

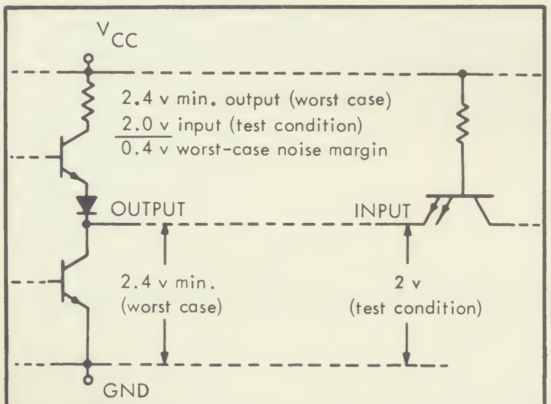


Figure C — Logical 1 Noise Margin

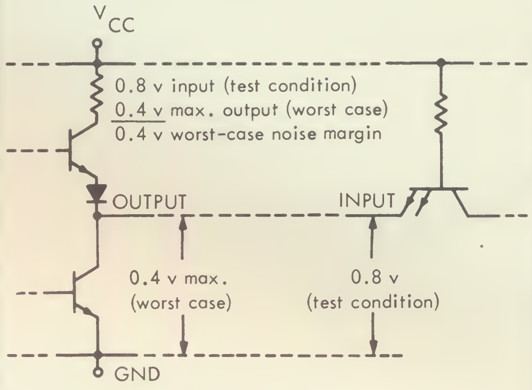


Figure D — Logical O Noise Margin

Each output is tested over the full temperature range to ensure that the logical 1 output voltage will not fall below 2.4 volts. This is done with full fan-out, lowest V_{CC}, and 0.8 volts on the input — 400 mv more than the logical 0 maximum.

Each output is tested over the full temperature range to ensure that the logical 0 output voltage will not exceed 0.4 volts. This is done with full fan-out, lowest V_{CC}, and 2 volts on the input — 400 mv less than the logical 1 minimum.

In actual system operation, the majority of circuits do not experience worst-case conditions of fan-out, supply voltage, temperature, and input voltage simultaneously. In addition, the threshold voltage of the Series 54 circuits is about 1.5 volts. These characteristics allow a larger voltage change on an input without false triggering. This typical noise margin is shown in figure E.

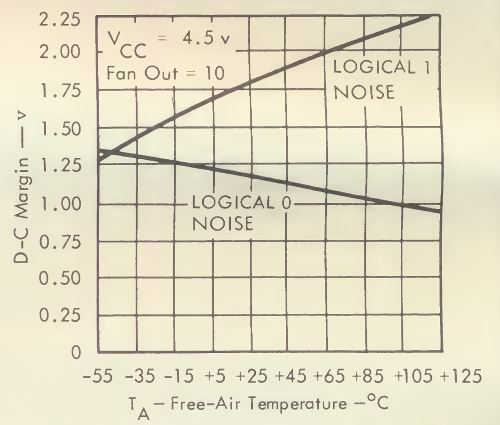


Figure E — Typical D-C Margin vs Temperature

Another important feature of the design is the output configuration which both supplies current (in the logical 1 state) and sinks current (in the logical 0 state) from a low impedance. Typically, logical 0 output impedance is 12 Ω and logical 1 output impedance is 100 Ω. This low output impedance in either state rejects capacitively coupled a-c pulses and ensures small R-C time constants which preserve waveshape integrity.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage, V_{CC} (See Note 1)	8 v
Input Voltage, V_{in} (See Notes 1 and 2)	5.5 v
Operating Free-Air Temperature Range	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

logic definition

Series 54 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

LOW VOLTAGE = LOGICAL 0

HIGH VOLTAGE = LOGICAL 1

input-current requirements

Input-current requirements reflect worst-case conditions for T_A = –55°C to 125°C and V_{CC} = 4.5 to 5.5 v. Each input of the multiple-emitter input transistor requires that no more than 1.6 ma flow out of the input at a logical 0 voltage level; therefore, one load (N = 1) is 1.6 ma maximum. The flip-flop preset and clear inputs supply two multiple-emitter transistors; thus, each preset or clear input is the equivalent of N = 2 loads. Each input requires current into the input at a logical 1 voltage level. This current is 40 μa maximum for all inputs except for the preset and clear which are 80 μa maximum.

fan-out capability

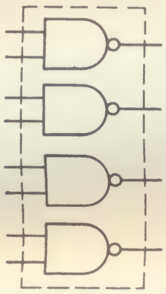
Fan-out reflects the ability of an output to sink current from a number of loads (N) at a logical 0 voltage level and to supply current at a logical 1 voltage level. Each output is capable of sinking current or supplying current to 10 loads (N = 10). The "power" gate is capable of sinking current or supplying current to 30 loads (N = 30).

unused inputs

All unused inputs except J★ and K★ should be connected to V_{CC}. Unused J★ or K★ input should be connected to ground.

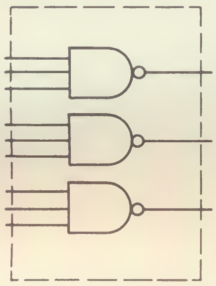
standard line summary

SN5400 See page 4



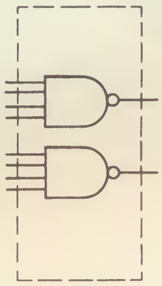
QUADRUPLE 2-INPUT POSITIVE NAND GATE

SN5410 See page 5



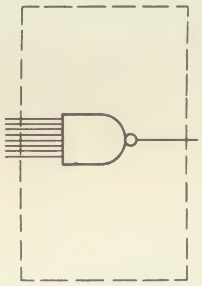
TRIPLE 3-INPUT POSITIVE NAND GATE

SN5420 See page 6



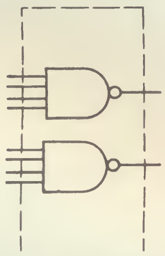
DUAL 4-INPUT POSITIVE NAND GATE

SN5430 See page 7



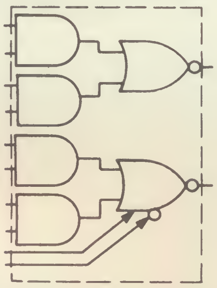
8-INPUT POSITIVE NAND GATE

SN5440 See page 8



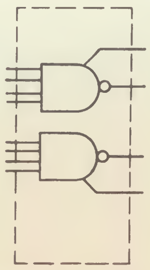
DUAL 4-INPUT POSITIVE NAND "POWER" GATE

SN5450 See page 9



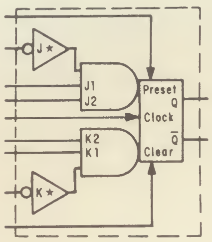
EXPANDABLE DUAL EXCLUSIVE-OR GATE

SN5460 See page 11



DUAL 4-INPUT EXPANDER FOR SN5450

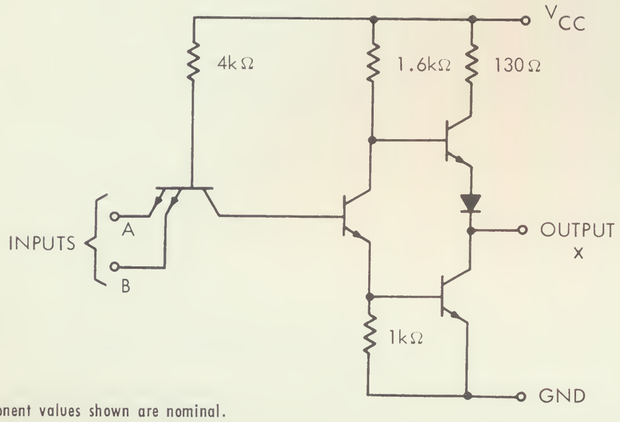
SN5470 See page 12



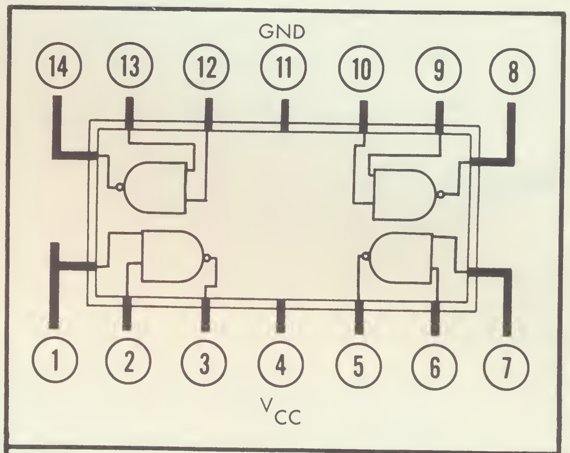
J-K FLIP-FLOP

TYPE SN5400
QUADRUPLE 2-INPUT POSITIVE NAND GATE

schematic (each gate)



Component values shown are nominal.



positive logic

$X = \overline{AB}$

recommended operating conditions

Supply Voltage, V_{CC} . . . . 4.5 v to 5.5 v

Maximum Fan-Out From Each Output, N 10

electrical characteristics, $T_A = -55°C$ to 125°C

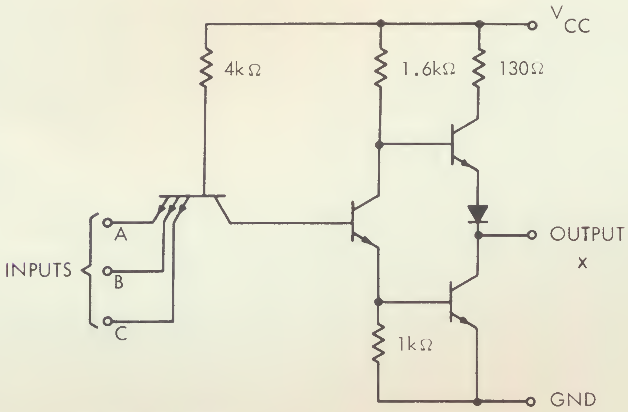
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals that will ensure logical 0 level at output	1	$V_{CC} = 4.5$ v, $V_{out(0)} \le 0.4$ v, $R = 256\ \Omega$	2			v
$V_{in(0)}$	Logical 0 input voltage required at any input terminal that will ensure logical 1 level at output	2	$V_{CC} = 4.5$ v, $V_{out(1)} \ge 2.4$ v, $R = 6\ k\Omega$			0.8	v
$V_{out(1)}$	Logical 1 output voltage	2	$V_{CC} = 4.5$ v, $V_{in} = 0.8$ v, $I_{load} \ge 400\ \mu a$, $R = 6\ k\Omega$	2.4			v
$V_{out(0)}$	Logical 0 output voltage	1	$V_{CC} = 4.5$ v, $V_{in} = 2$ v, $I_{sink} \ge 16$ ma, $R = 256\ \Omega$			0.4	v
I_{in}	Input current (each input)	3	$V_{CC} = 5.5$ v, $V_{in} = 0.4$ v			1.6	ma
I_{in}	Input current (each input)	4	$V_{CC} = 5.5$ v, $V_{in} = 4.5$ v			40	μa
I_{OS}	Short-circuit output current†	5	$V_{CC} = 5.5$ v	20		55	ma
$I_{CC(0)}$	Logical 0 level supply current (each gate)	6	$V_{CC} = V_{in} = 5$ v		3		ma
$I_{CC(1)}$	Logical 1 level supply current (each gate)	6	$V_{CC} = 5$ v, $V_{in} = 0$		1		ma

switching characteristics, $V_{CC} = 5$ v, $T_A = 25°C$

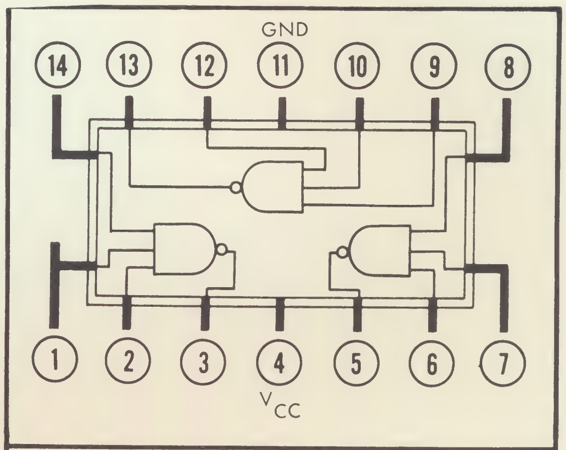
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d0}	Propagation time to logical 0	27	$C_1 = 15$ pf, $N = 10$		8	15	nsec
t_{d1}	Propagation time to logical 1	27	$C_1 = 15$ pf, $N = 1$		18	29	nsec

†Not more than one output should be shorted at a time.

schematic (each gate)



Component values shown are nominal.



positive logic

$X = \overline{ABC}$

recommended operating conditions

Supply Voltage, V_{CC} . . . . 4.5 v to 5.5 v

Maximum Fan-Out From Each Output, N 10

electrical characteristics, $T_A = -55°C$ to $125°C$

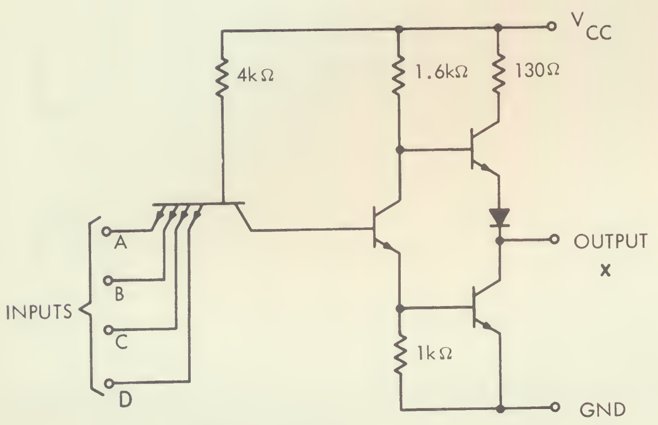
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals that will ensure logical 0 level at output	1	$V_{CC} = 4.5$ v, $V_{out(0)} \leq 0.4$ v, $R = 256\ \Omega$	2			v
$V_{in(0)}$	Logical 0 input voltage required at any input terminal that will ensure logical 1 level at output	2	$V_{CC} = 4.5$ v, $V_{out(1)} \geq 2.4$ v, $R = 6\ k\Omega$			0.8	v
$V_{out(1)}$	Logical 1 output voltage	2	$V_{CC} = 4.5$ v, $V_{in} = 0.8$ v, $I_{load} \geq 400\ \mu a$, $R = 6\ k\Omega$	2.4			v
$V_{out(0)}$	Logical 0 output voltage	1	$V_{CC} = 4.5$ v, $V_{in} = 2$ v, $I_{sink} \geq 16$ ma, $R = 256\ \Omega$			0.4	v
I_{in}	Input current (each input)	3	$V_{CC} = 5.5$ v, $V_{in} = 0.4$ v			1.6	ma
I_{in}	Input current (each input)	4	$V_{CC} = 5.5$ v, $V_{in} = 4.5$ v			40	μa
I_{OS}	Short-circuit output current†	5	$V_{CC} = 5.5$ v	20		55	ma
$I_{CC(0)}$	Logical 0 level supply current (each gate)	6	$V_{CC} = V_{in} = 5$ v		3		ma
$I_{CC(1)}$	Logical 1 level supply current (each gate)	6	$V_{CC} = 5$ v, $V_{in} = 0$		1		ma

switching characteristics, $V_{CC} = 5$ v, $T_A = 25°C$

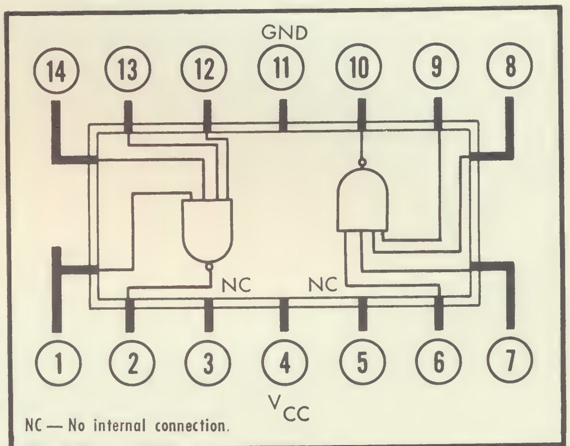
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d0}	Propagation time to logical 0	27	$C_1 = 15$ pf, $N = 10$		8	15	nsec
t_{d1}	Propagation time to logical 1	27	$C_1 = 15$ pf, $N = 1$		18	29	nsec

†Not more than one output should be shorted at a time.

schematic (each gate)



Component values shown are nominal.



positive logic

$X = \overline{ABCD}$

recommended operating conditions

Supply Voltage, V_{CC} . . . . 4.5 v to 5.5 v

Maximum Fan-Out From Each Output, N 10

electrical characteristics $T_A = -55°C$ to $125°C$

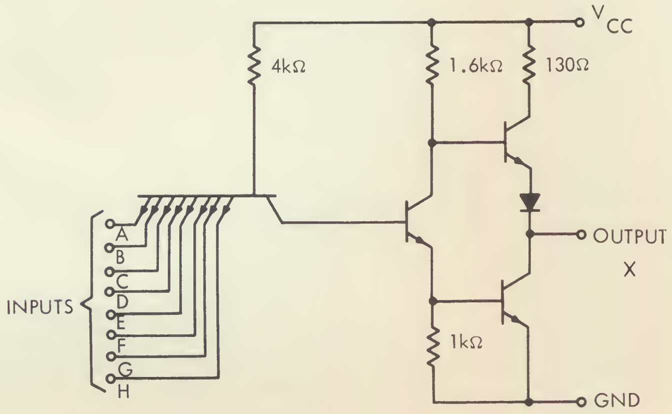
	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals that will ensure logical 0 level at output	1	$V_{CC} = 4.5$ v, $V_{out(0)} \leq 0.4$ v, $R = 256\ \Omega$	2			v
$V_{in(0)}$	Logical 0 input voltage required at any input terminal that will ensure logical 1 level at output	2	$V_{CC} = 4.5$ v, $V_{out(1)} \geq 2.4$ v, $R = 6\ k\Omega$			0.8	v
$V_{out(1)}$	Logical 1 output voltage	2	$V_{CC} = 4.5$ v, $V_{in} = 0.8$ v, $I_{load} \geq 400\ \mu a$, $R = 6\ k\Omega$	2.4			v
$V_{out(0)}$	Logical 0 output voltage	1	$V_{CC} = 4.5$ v, $V_{in} = 2$ v, $I_{sink} \geq 16$ ma, $R = 256\ \Omega$			0.4	v
I_{in}	Input current (each input)	3	$V_{CC} = 5.5$ v, $V_{in} = 0.4$ v			1.6	ma
I_{in}	Input current (each input)	4	$V_{CC} = 5.5$ v, $V_{in} = 4.5$ v			40	μa
I_{OS}	Short-circuit output current†	5	$V_{CC} = 5.5$ v	20		55	ma
$I_{CC(0)}$	Logical 0 level supply current (each gate)	6	$V_{CC} = V_{in} = 5$ v		3		ma
$I_{CC(1)}$	Logical 1 level supply current (each gate)	6	$V_{CC} = 5$ v, $V_{in} = 0$		1		ma

switching characteristics, $V_{CC} = 5$ v, $T_A = 25°C$

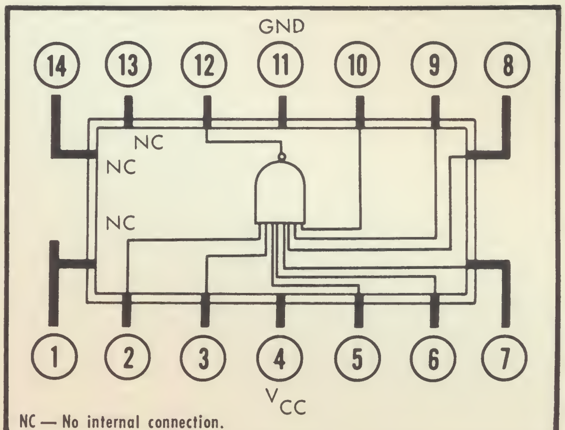
	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d0}	Propagation time to logical 0	27	$C_1 = 15$ pf, $N = 10$		8	15	nsec
t_{d1}	Propagation time to logical 1	27	$C_1 = 15$ pf, $N = 1$		18	29	nsec

†Not more than one output should be shorted at a time.

schematic (each gate)



Component values shown are nominal.



NC — No internal connection.

positive logic

$X = \overline{ABCDEFGH}$

recommended operating conditions

Supply Voltage, V_{CC} . . . . 4.5 v to 5.5 v

Maximum Fan-Out From Each Output, N 10

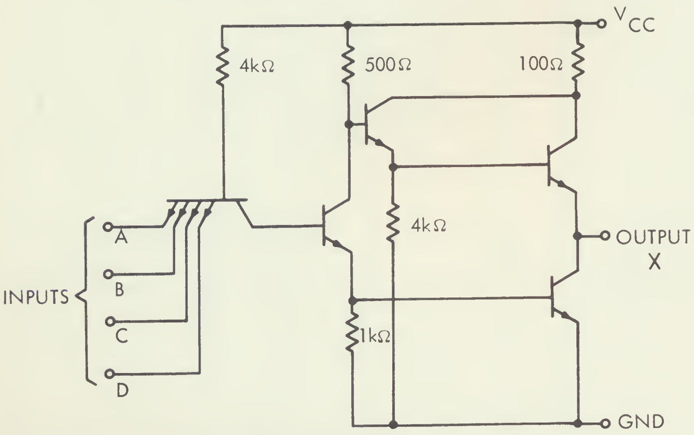
electrical characteristics, $T_A = -55°C$ to $125°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals that will ensure logical 0 level at output	1	$V_{CC} = 4.5$ v, $V_{out(0)} \leq 0.4$ v, $R = 256\ \Omega$	2			v
$V_{in(0)}$	Logical 0 input voltage required at any input terminal that will ensure logical 1 level at output	2	$V_{CC} = 4.5$ v, $V_{out(1)} \geq 2.4$ v, $R = 6\ k\Omega$			0.8	v
$V_{out(1)}$	Logical 1 output voltage	2	$V_{CC} = 4.5$ v, $V_{in} = 0.8$ v, $I_{load} \geq 400\ \mu a$, $R = 6\ k\Omega$	2.4			v
$V_{out(0)}$	Logical 0 output voltage	1	$V_{CC} = 4.5$ v, $V_{in} = 2$ v, $I_{sink} \geq 16$ ma, $R = 256\ \Omega$			0.4	v
I_{in}	Input current (each input)	3	$V_{CC} = 5.5$ v, $V_{in} = 0.4$ v			1.6	ma
I_{in}	Input current (each input)	4	$V_{CC} = 5.5$ v, $V_{in} = 4.5$ v			40	μa
I_{OS}	Short-circuit output current	5	$V_{CC} = 5.5$ v	20		55	ma
$I_{CC(0)}$	Logical 0 level supply current (each gate)	6	$V_{CC} = V_{in} = 5$ v		3		ma
$I_{CC(1)}$	Logical 1 level supply current (each gate)	6	$V_{CC} = 5$ v, $V_{in} = 0$		1		ma

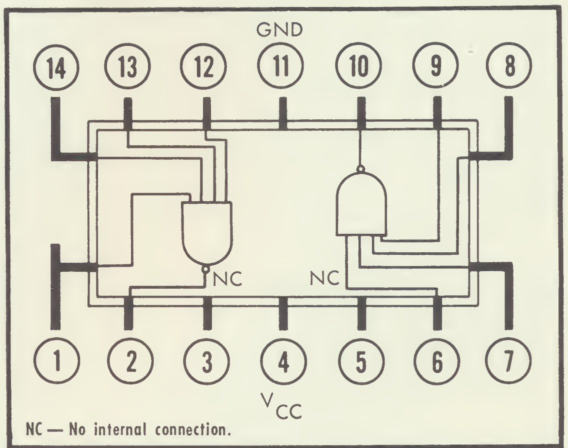
switching characteristics, $V_{CC} = 5$ v, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d0}	Propagation time to logical 0	27	$C_1 = 15$ pf, $N = 10$		8	15	nsec
t_{d1}	Propagation time to logical 1	27	$C_1 = 15$ pf, $N = 1$		18	29	nsec

schematic (each gate)



Component values shown are nominal.



positive logic

$X = \overline{ABCD}$

recommended operating conditions

Supply Voltage, V_{CC} . . . . 4.5 to 5.5 v
Maximum Fan-Out From Each Output, N 30

electrical characteristics, $T_A = -55°C$ to 125°C

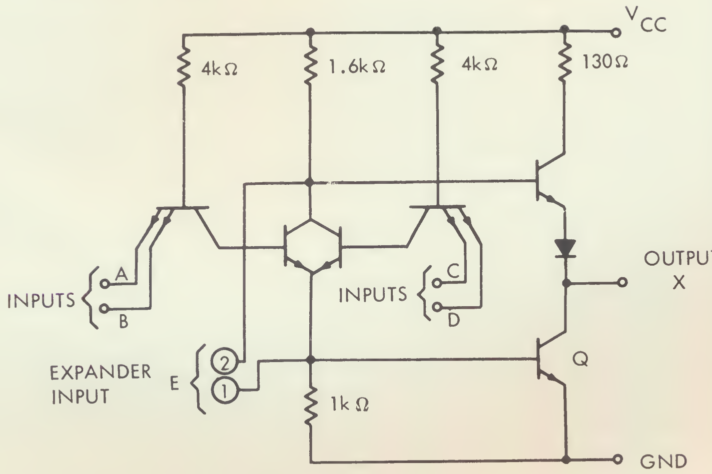
	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals that will ensure logical 0 level at output	1	$V_{CC} = 4.5$ v, $V_{out(0)} \leq 0.4$ v, $R = 85\ \Omega$	2			v
$V_{in(0)}$	Logical 0 input voltage required at any input terminal that will ensure logical 1 level at output	2	$V_{CC} = 4.5$ v, $V_{out(1)} \geq 2.4$ v, $R = 2\ k\Omega$			0.8	v
$V_{out(1)}$	Logical 1 output voltage	2	$V_{CC} = 4.5$ v, $V_{in} = 0.8$ v, $I_{load} \geq 1.2$ ma, $R = 2\ k\Omega$	2.4			v
$V_{out(0)}$	Logical 0 output voltage	1	$V_{CC} = 4.5$ v, $V_{in} = 2$ v, $I_{sink} \geq 48$ ma, $R = 85\ \Omega$			0.4	v
I_{in}	Input current (each input)	3	$V_{CC} = 5.5$ v, $V_{in} = 0.4$ v			1.6	ma
I_{in}	Input current (each input)	4	$V_{CC} = 5.5$ v, $V_{in} = 4.5$ v			40	μa
I_{OS}	Short-circuit output current†	5	$V_{CC} = 5.5$ v	20		70	ma
$I_{CC(0)}$	Logical 0 level supply current (each gate)	6	$V_{CC} = V_{in} = 5$ v		8.6		ma
$I_{CC(1)}$	Logical 1 level supply current (each gate)	6	$V_{CC} = 5$ v, $V_{in} = 0$		2		ma

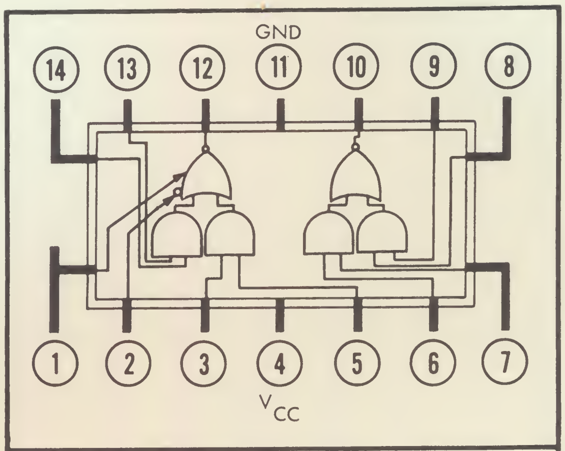
switching characteristics, $V_{CC} = 5$ v, $T_A = 25°C$

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d0}	Propagation time to logical 0	27	$C_1 = 15$ pf, $N = 30$		8	15	nsec
t_{d1}	Propagation time to logical 1	27	$C_1 = 15$ pf, $N = 1$		18	29	nsec

†Not more than one output should be shorted at a time.

schematic (each gate)





positive logic

$X = \overline{(AB) + (CD) + E}$

$E = ABCD$ from SN5460

NOTES: 1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding with the SN5460.
3. If expander is not used leave pins ① and ② open.

recommended operating conditions

Supply Voltage, V_{CC} . . . . 4.5 v to 5.5 v

Maximum Fan-Out From Each Output, N 10

electrical characteristics, $T_A = -55°C$ to $125°C$, pins ① and ② open

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section that will ensure logical 0 at output	7	$V_{CC} = 4.5$ v, $V_{out(0)} \leq 0.4$ v, $R = 256\ \Omega$	2			v
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section that will ensure logical 1 at output	8	$V_{CC} = 4.5$ v, $V_{out(1)} \geq 2.4$ v, $R = 6\ k\Omega$			0.8	v
$V_{out(1)}$	Logical 1 output voltage	8	$V_{CC} = 4.5$ v, $V_{in} = 0.8$ v, $I_{load} \geq 400\ \mu a$, $R = 6\ k\Omega$	2.4			v
$V_{out(0)}$	Logical 0 output voltage	7	$V_{CC} = 4.5$ v, $V_{in} = 2$ v, $I_{sink} \geq 16$ ma, $R = 256\ \Omega$			0.4	v
I_{in}	Input current (each input)	9	$V_{CC} = 5.5$ v, $V_{in} = 4.5$ v			1.6	ma
I_{in}	Input current (each input)	10	$V_{CC} = 5.5$ v, $V_{in} = 0$			40	μa
I_{OS}	Short-circuit output current†	11	$V_{CC} = 5.5$ v	20		55	ma
$I_{CC(0)}$	Logical 0 level supply current (each gate)	12	$V_{CC} = V_{in} = 5$ v		3.7		ma
$I_{CC(1)}$	Logical 1 level supply current (each gate)	13	$V_{CC} = 5$ v, $V_{in} = 0$		2		ma

†Not more than one output should be shorted at a time.

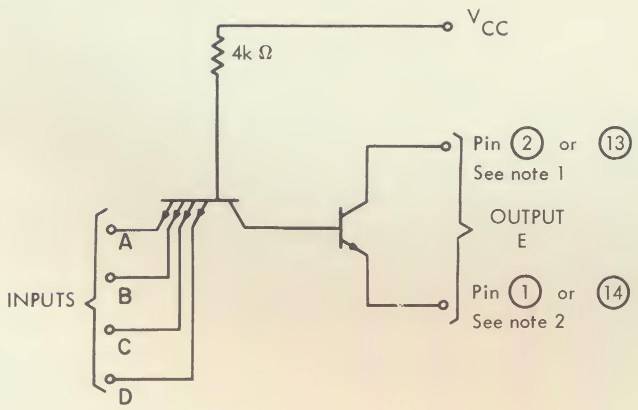
electrical characteristics using expander inputs, $T_A = -55°C$

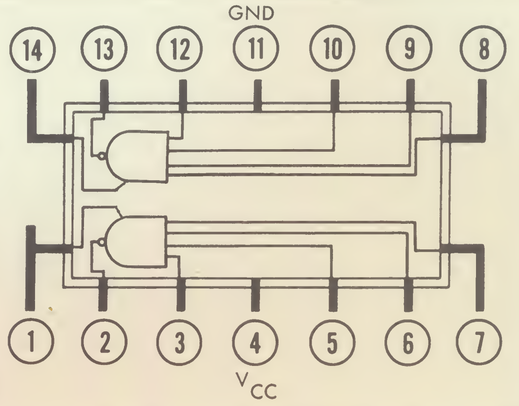
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{(X)}$	Expander current	14	$V_{CC} = 4.5$ v, $V_1 = 0.4$ v, $I_{sink} = 16$ ma,	1.5	2.9	ma
$V_{BE(Q)}$	Output transistor (Q) base-emitter voltage	15	$V_{CC} = 4.5$ v, $V_2 = 1.4$ v, $I_{sink} = 16$ ma, $I_1 = 1.7$ ma, $R = 256\ \Omega$		1	v
$V_{out(0)}$	Logical 0 output voltage	15	$V_{CC} = 4.5$ v, $V_2 = 1.4$ v, $I_{sink} = 16$ ma, $I_1 = 1.7$ ma, $R = 256\ \Omega$		0.4	v
$V_{out(1)}$	Logical 1 output voltage	16	$V_{CC} = 4.5$ v, $I_{load} = 400\ \mu a$, $I_1 = 0.15$ ma, $I_2 = 0.15$ ma, $R = 6\ k\Omega$	2.4		v

switching characteristics, $V_{CC} = 5$ v, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d0}	Propagation time to logical 0	27	$C_1 = 15$ pf, $N = 10$		8	15	nsec
t_{d1}	Propagation time to logical 1	27	$C_1 = 15$ pf, $N = 1$		18	29	nsec

schematic





positive logic
E = ABCD
When connected to pins 1 and 2 of SN5450

NOTES: 1. Connect pin 2 or 13 to pin 2 of SN5450.
2. Connect pin 1 or 14 to pin 1 of SN5450.
3. Component values shown are nominal.

recommended operating conditions

Supply Voltage, V_{CC} . . . . . 4.5 v to 5.5 v
Maximum number of expanders that may be fanned-in to one SN5450 4

electrical characteristics (unless otherwise noted $T_A = -55°C$ to $125°C$)

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals that will ensure output on level	17	$V_{CC} = 4.5$ v, $V_{in} = 2$ v, $V_1 = 1$ v, $R = 1.1$ kΩ, $T_A = -55°C$	2			v
$V_{in(0)}$	Logical 0 input voltage at any input terminal that will ensure output off level current	18	$V_{CC} = 4.5$ v, $V_{in} = 0.8$ v, $V_1 = 4.5$ v, $R = 1.2$ kΩ, $I_{off} = 0.15$ ma, $T_A = -55°C$			0.8	v
V_{on}	Output voltage on level	17	$V_{CC} = 4.5$ v, $V_{in} = 2$ v, $V_1 = 1$ v, $R = 1.1$ kΩ, $T_A = -55°C$			0.4	v
I_{off}	Output off level current	18	$V_{CC} = 4.5$ v, $V_{in} = 0.8$ v, $V_1 = 4.5$ v, $R = 1.2$ kΩ, $T_A = -55°C$			150	μa
I_{on}	Output on level current	19	$V_{CC} = 4.5$ v, $V_{in} = 2$ v, $V_1 = 1$ v, $I_2 = 1.5$ ma	1.7			ma
I_{in}	Input current (each input)	18	$V_{CC} = 5.5$ v, $V_{in} = 0.4$ v			1.6	ma
I_{in}	Input current (each input)	20	$V_{CC} = 5.5$ v, $V_{in} = 4.5$ v, $T_A = 125°C$			40	μa
$I_{CC(on)}$	On level supply current (each gate)	21	$V_{CC} = V_{in} = 5$ v, $V_1 = 0.85$ v		0.6		ma
$I_{CC(off)}$	Off level supply current (each gate)	21	$V_{CC} = 5$ v, $V_{in} = 0$, $V_1 = 0.85$ v		1		ma

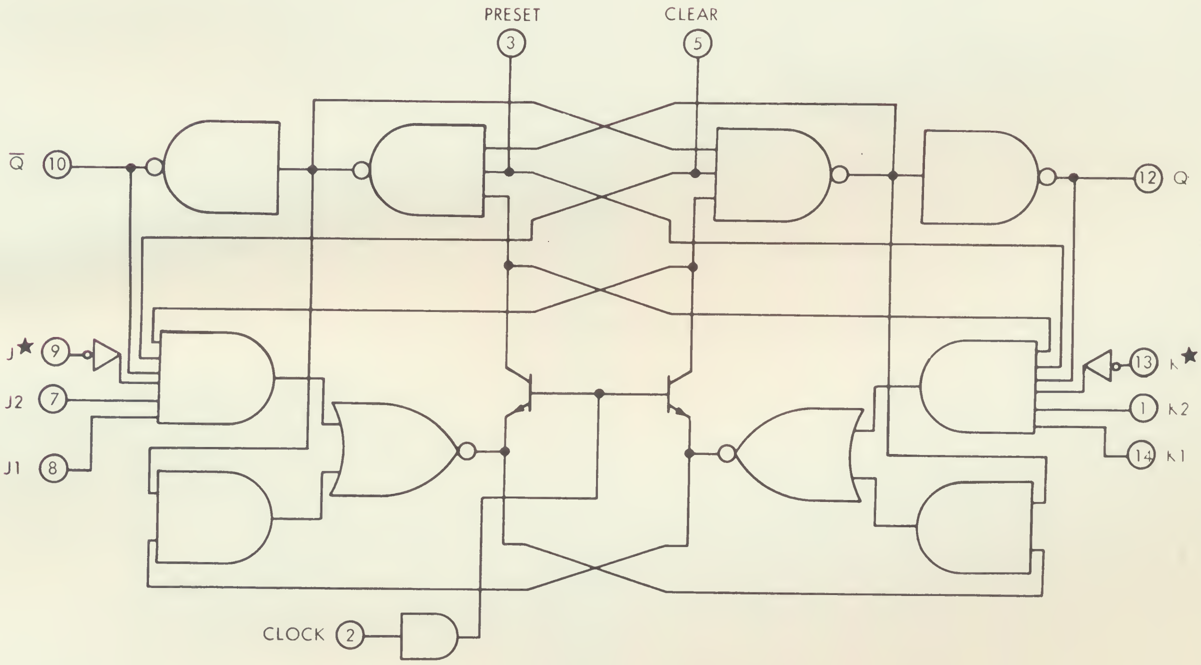
switching characteristics, $V_{CC} = 5$ v, $T_A = 25°C$

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d0}	Propagation time to logical 0 (through SN5450)	28	$C_1 = 15$ pf, $N = 10$		10	20	nsec
t_{d1}	Propagation time to logical 1 (through SN5450)	28	$C_1 = 15$ pf, $N = 1$		20	34	nsec

switching characteristics, $V_{CC} = 5$ v, $T_A = 25°C$

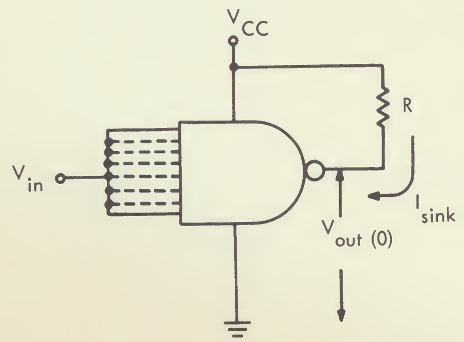
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{set\text{-}up}$	Minimum Input Set-Up Time	29			15		nsec
t_{hold}	Minimum Input Hold Time				10		nsec
t_{preset}	Minimum Preset Time	30			15		nsec
t_{clear}	Minimum Clear Time				15		nsec
t_{d0}	Propagation time to logical 0	29	$C_1 = 15$ pf, $N = 10$		30	50	nsec
t_{d1}	Propagation time to logical 1	29	$C_1 = 15$ pf, $N = 1$		30	50	nsec

functional block diagram



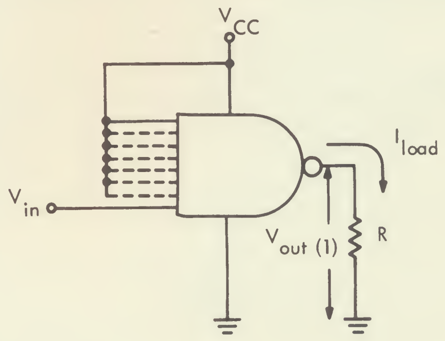
PARAMETER MEASUREMENT INFORMATION

d-c test circuits



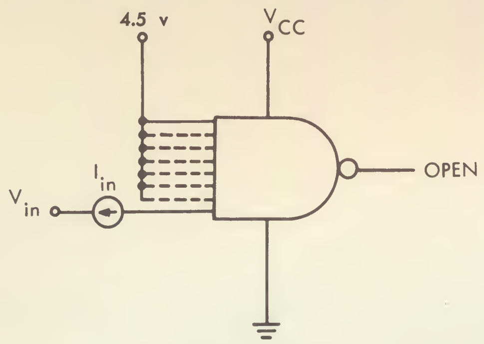
1. All inputs tested simultaneously.

FIGURE 1



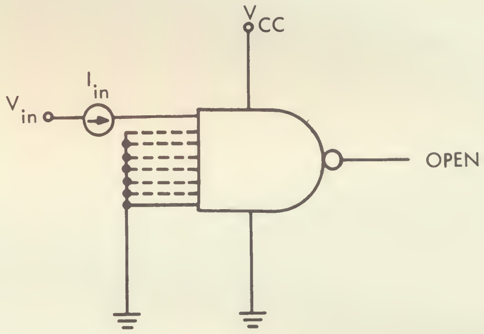
1. Each input tested separately.

FIGURE 2



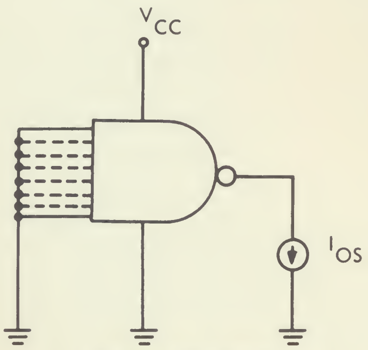
1. Each input tested separately.

FIGURE 3



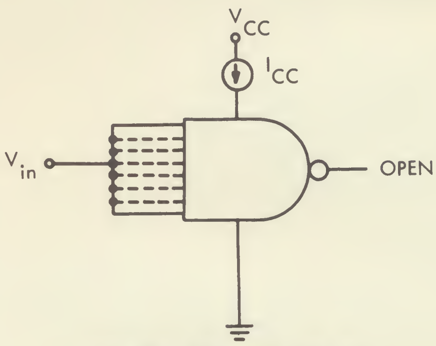
1. Each input tested separately.

FIGURE 4



1. Each gate tested separately.

FIGURE 5

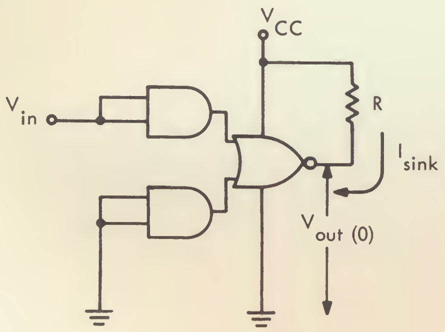


1. Test logical 0 and logical 1 conditions.

FIGURE 6

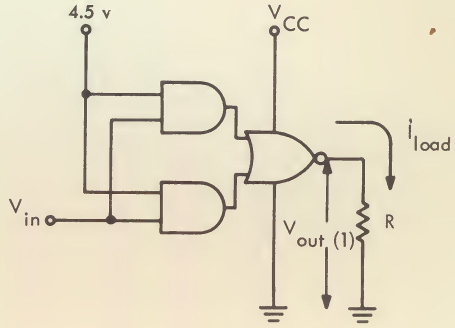
PARAMETER MEASUREMENT INFORMATION

d-c test circuits (continued)



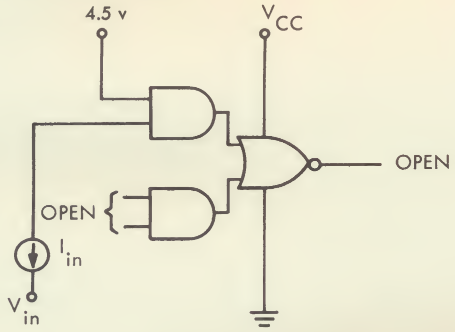
1. Each AND section tested separately.

FIGURE 7



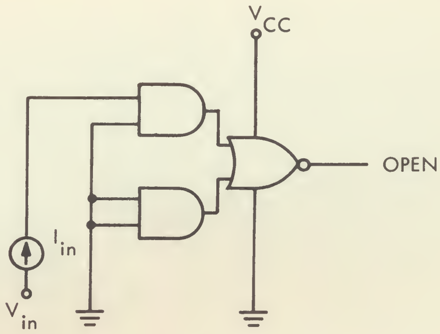
1. Each pair of inputs tested separately.

FIGURE 8



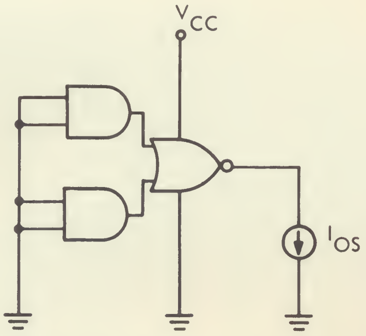
1. Each input tested separately.

FIGURE 9



1. Each input tested separately.

FIGURE 10



1. Each gate tested separately.

FIGURE 11

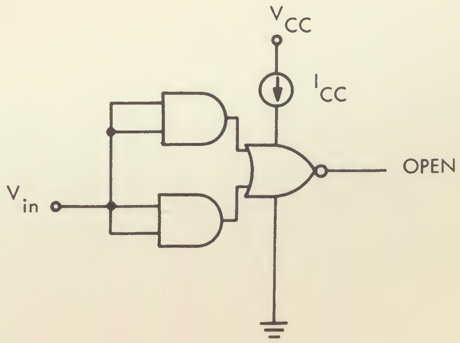


FIGURE 12

PARAMETER MEASUREMENT INFORMATION

d-c test circuits (continued)

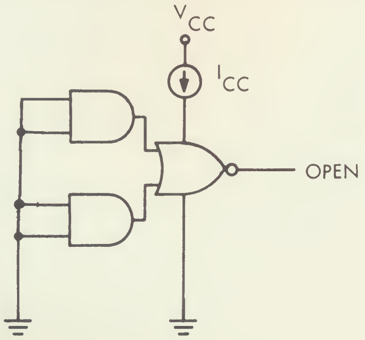


FIGURE 13

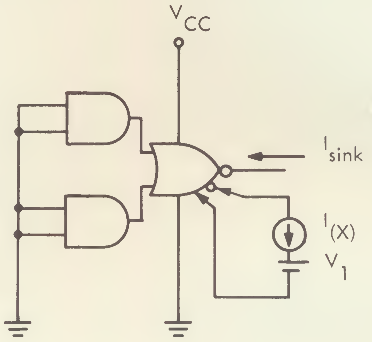


FIGURE 14

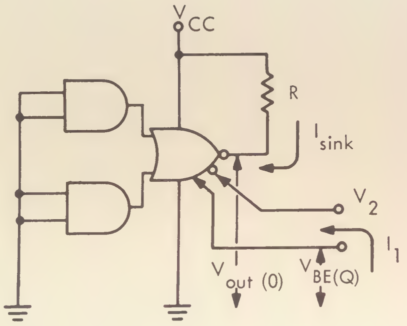


FIGURE 15

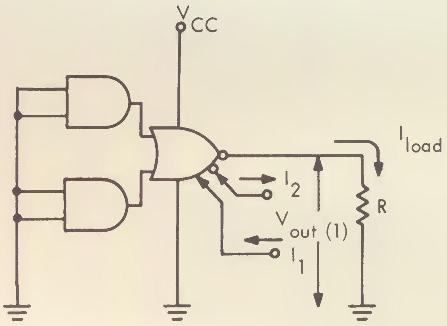
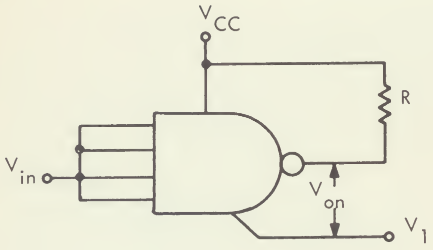
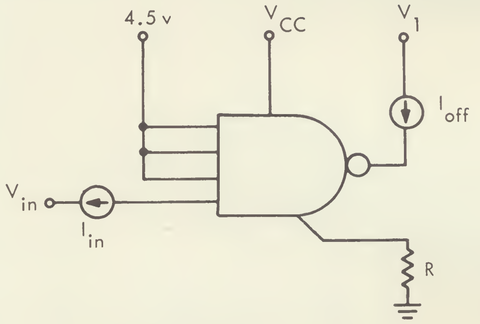


FIGURE 16



1. All inputs tested simultaneously.

FIGURE 17



1. Each input tested separately.

FIGURE 18

PARAMETER MEASUREMENT INFORMATION

d-c test circuits (continued)

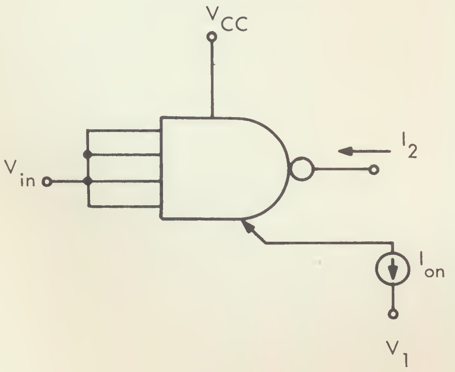
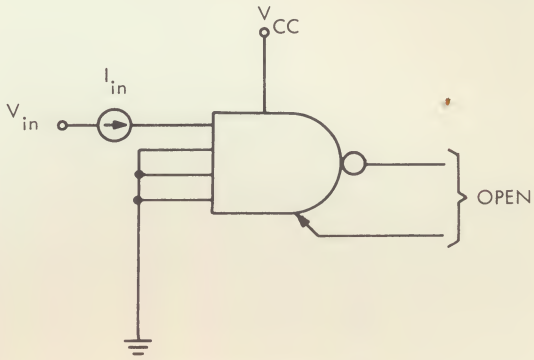
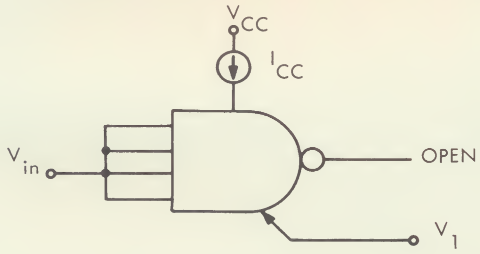


FIGURE 19



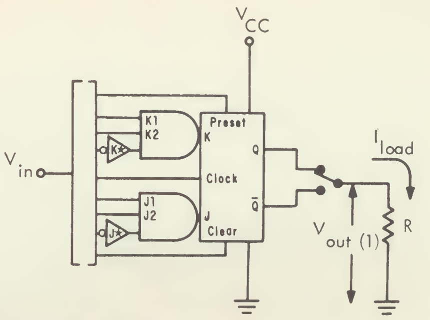
1. Each input tested separately.

FIGURE 20



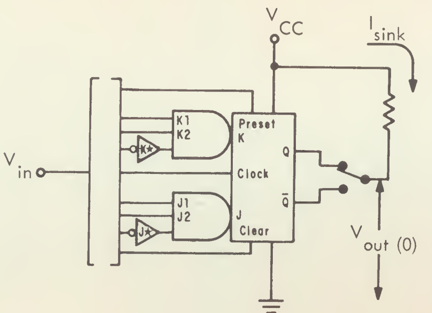
1. Test "on" and "off" conditions.

FIGURE 21



1. Each output is tested separately.
2. The flip-flop is tested to ensure conformance to truth table.
3. Preset and clear are tested with $V_{in(clock)} = 0$.
4. All unused inputs are connected to worst case voltages.

FIGURE 22

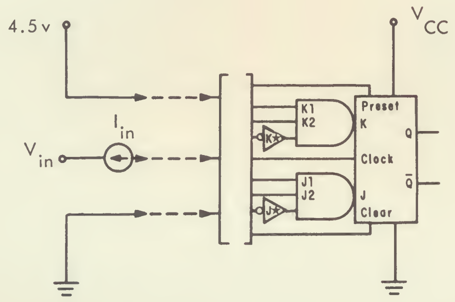


1. Each output is tested separately.

FIGURE 23

PARAMETER MEASUREMENT INFORMATION

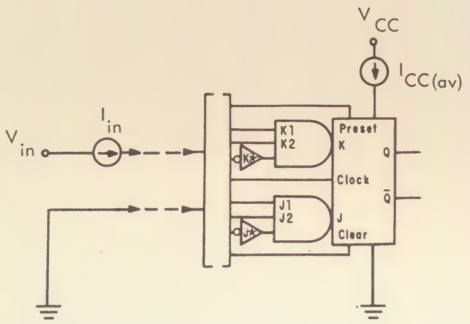
d-c test circuits (continued)



TEST TABLE		
Apply V_{in} (Test I_{in})	Apply 4.5 v	Ground
J2	J1	Clear
J1	J2	Clear
J★	None	None
K2	K1	Preset
K1	K2	Preset
K★	None	None
Clock	None	None
Preset	None	Clear
Clear	None	Preset

1. Each input is tested separately.

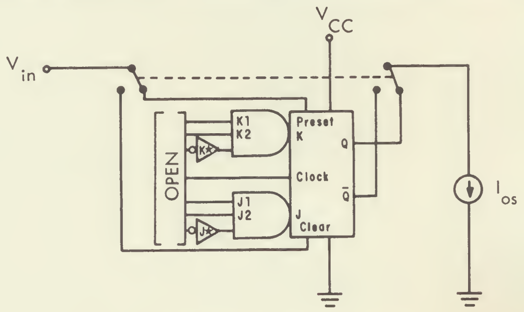
FIGURE 24



TEST TABLE (See Note 2)	
Apply V_{in} (Test I_{in})	Ground
J2	J1
J1	J2
J★	None
K2	K1
K1	K2
K★	None
Clock	None
Preset	(See Note 3)
Clear	(See Note 3)

1. Each input is tested separately.
2. Test voltage and grounds are applied to inputs in accordance with the test table, and I_{in} is measured for input being tested.
3. A momentary ground is applied to preset or clear prior to applying V_{in} and testing I_{in} at these two inputs.

FIGURE 25

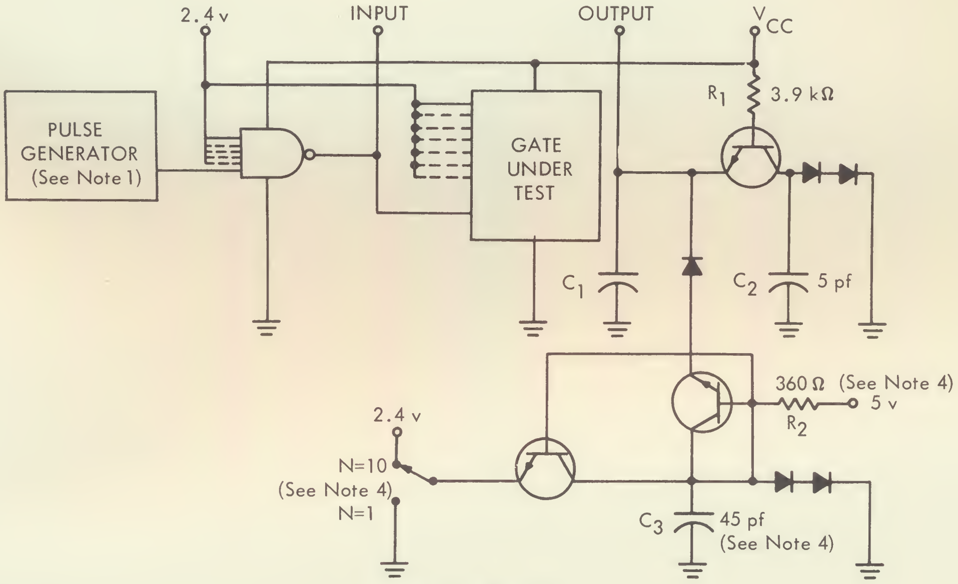


1. Each output is tested separately.

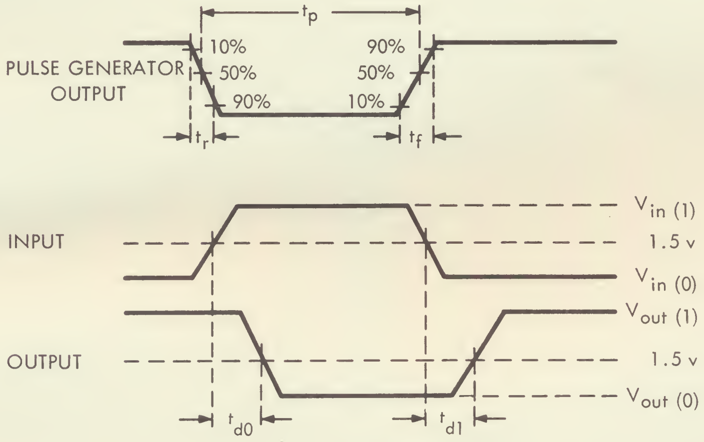
FIGURE 26

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



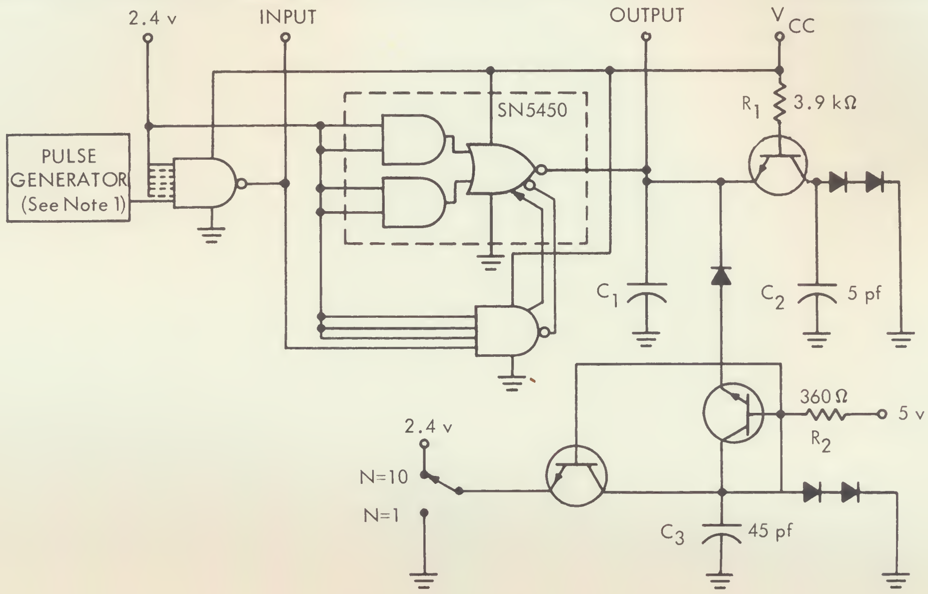
VOLTAGE WAVEFORMS

NOTES:
1. The generator has the following characteristics: $t_r = t_f \leq 15$ nsec, $t_p = 9.5$ μsec, PRR = 100 kc, $Z_{out} \approx 50\ \Omega$.
2. All transistors are 2N2368.
3. All diodes are IN916.
4. Test SN5440 with $R_2 = 100\ \Omega$, $C_3 = 145$ pf, N = 30 for t_{d0}, and N=1 for t_{d1}
5. $t_{pd} = \dfrac{t_{d0} + t_{d1}}{2}$

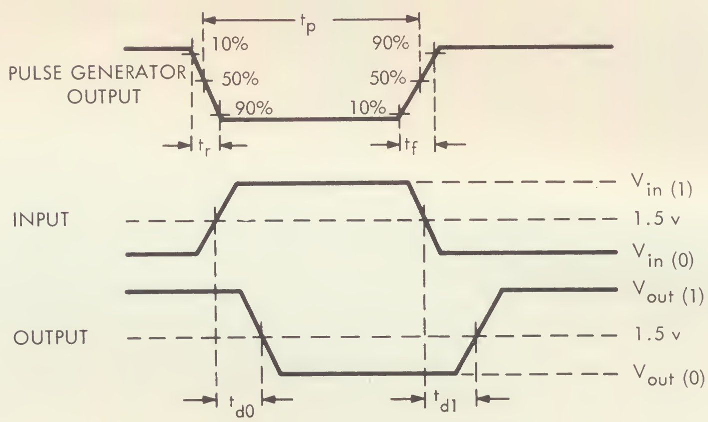
FIGURE 27 — GATE PROPAGATION DELAY

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics: $t_r = t_f \leq 15$ nsec, $t_p = 9.5\ \mu$sec, PRR = 100 kc, $Z_{out} \approx 50\ \Omega$.

2. All transistors are 2N2368.

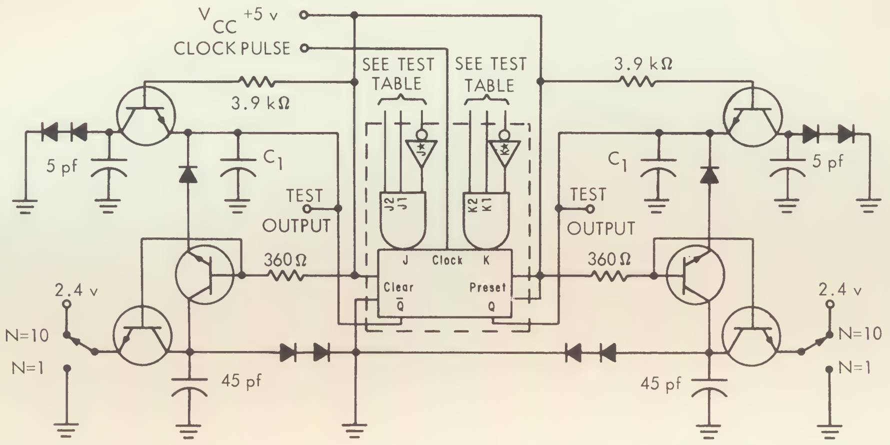
3. All diodes are 1N916.

4. $t_{pd} = \frac{t_{d0} + t_{d1}}{2}$

FIGURE 28 — EXPANDER PROPAGATION DELAY

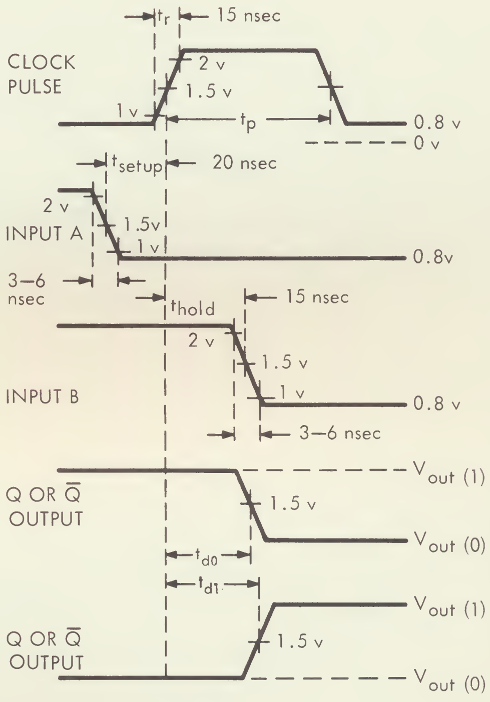
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT

TEST TABLE					
TEST NO.	TEST	INPUT A	INPUT B	+2.4 v	GND
1	t_{d0} ($\bar{Q}$)	J★	J1, J2	K1, K2	K★
2	t_{d1} ($\bar{Q}$)	K★	K1, K2	J1, J2	J★
3	t_{d0} (Q)	K★	K1, K2	J1, J2	J★
4	t_{d1} (Q)	J★	J1, J2	K1, K2	K★



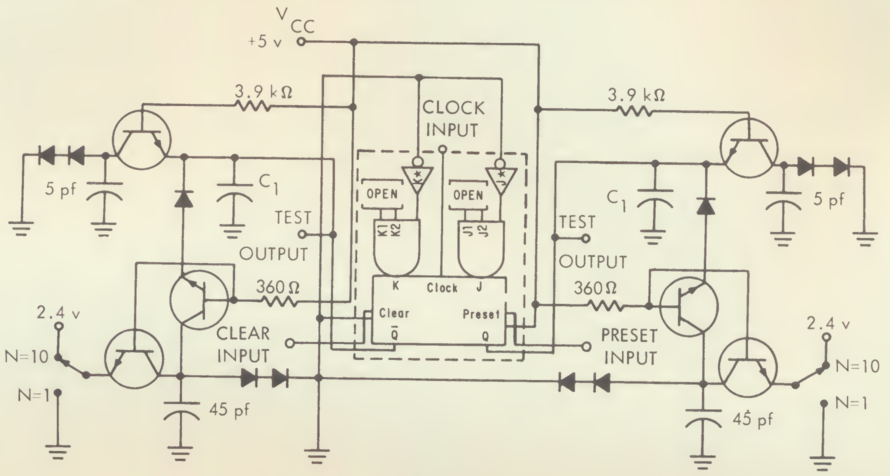
NOTES: 1. All transistors are 2N2368.
2. All diodes are 1N916.

VOLTAGE WAVEFORMS.

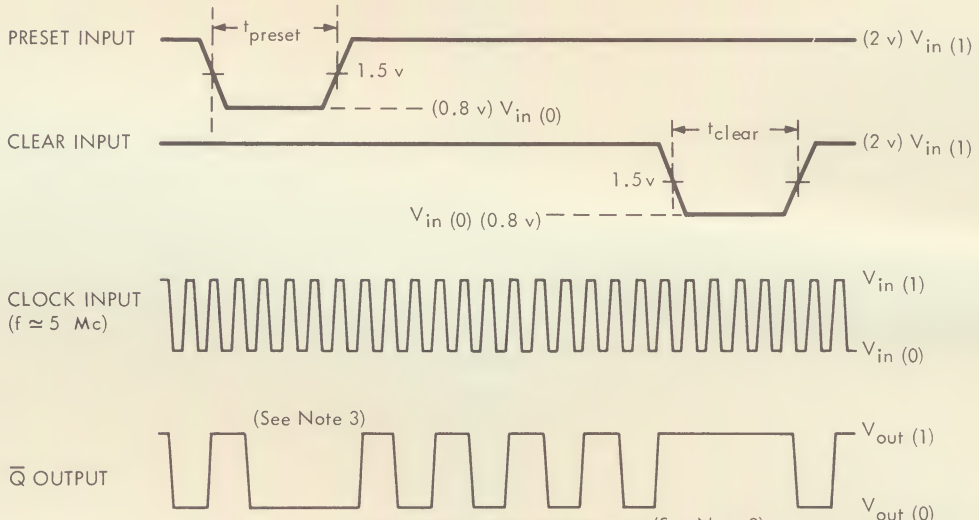
FIGURE 29 — FLIP-FLOP SWITCHING-TIME

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



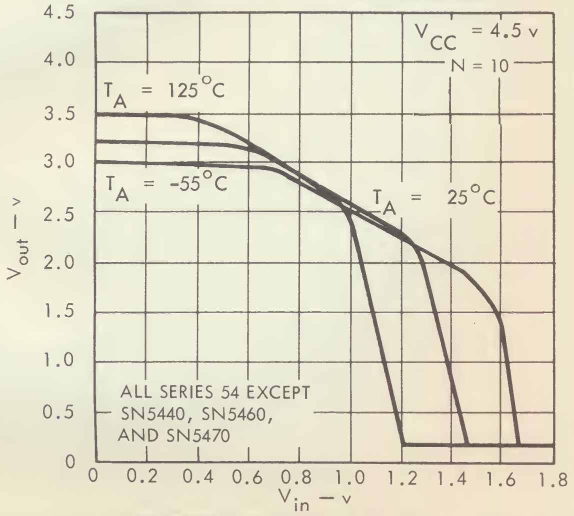
VOLTAGE WAVEFORMS (See Note 3)

NOTES:
1. All transistors are 2N2368.
2. All diodes are 1N916.
3. Clock input of 5 Mc is used to verify that preset or clear input inhibits the clock function.

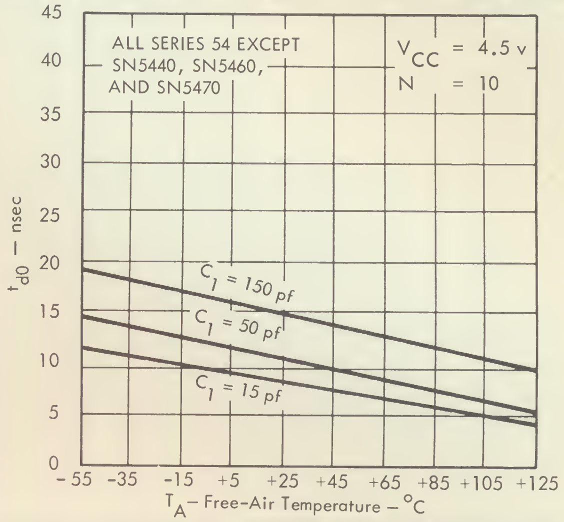
FIGURE 30 — PRESET/CLEAR

TYPICAL CHARACTERISTICS

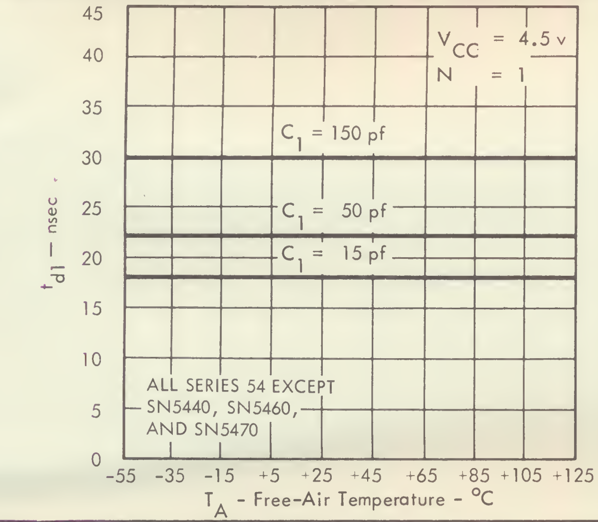
OUTPUT VOLTAGE vs INPUT VOLTAGE



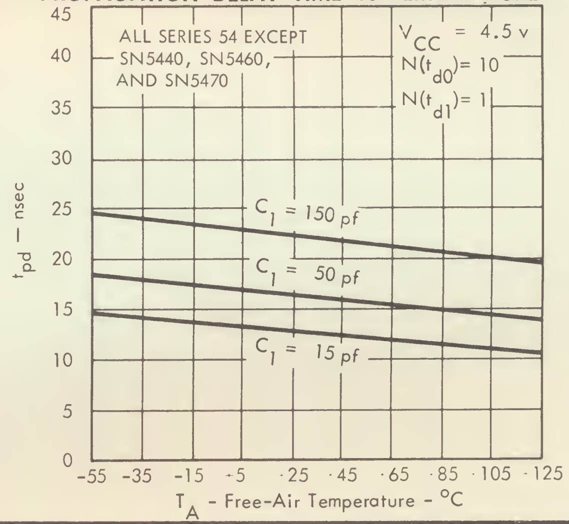
PROPAGATION TIME TO LOGICAL 0 vs TEMPERATURE



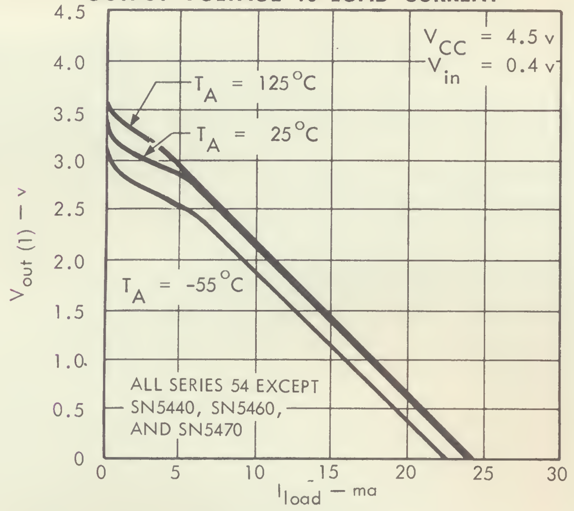
PROPAGATION TIME TO LOGICAL 1 vs TEMPERATURE



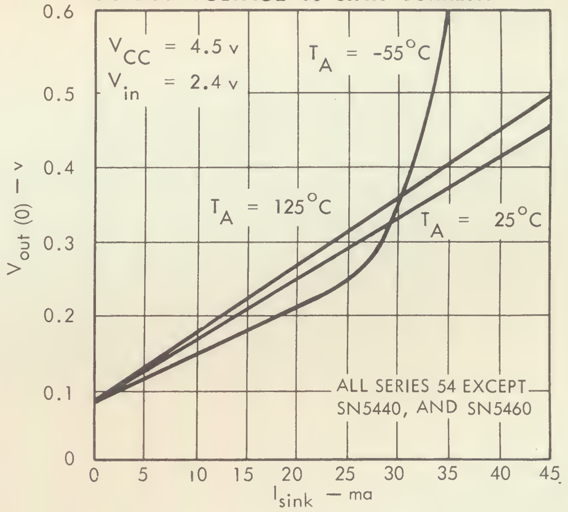
PROPAGATION DELAY TIME vs TEMPERATURE



OUTPUT VOLTAGE vs LOAD CURRENT



OUTPUT VOLTAGE vs SINK CURRENT

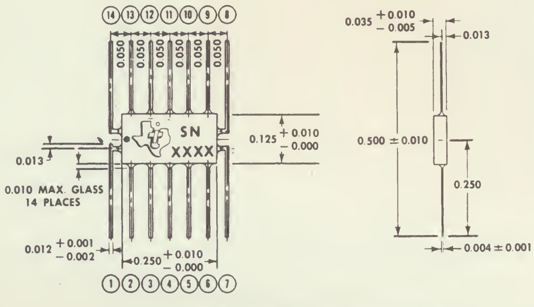


MECHANICAL DATA

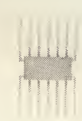
general

SOLID CIRCUIT semiconductor networks are mounted in a glass-to-metal hermetically sealed, welded package. Package body and leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. All Series 54 networks are available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier.

OUTLINE DRAWING — SEMICONDUCTOR NETWORK WELDED PACKAGE



NOTES: a. All dimensions in inches.
b. All decimals ±0.005 except as noted.
c. Lead spacing tolerance is ±0.015 at extremities and ±0.005 at package, nonaccumulative.
d. Lead centerlines are located within ±0.005 of their true positions relative to body centerlines.
e. Symbolization denotes orientation of package.

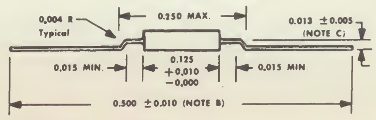


Falls Within TO-84 Dimensions

leads

Gold-plated F-15‡ leads require no additional cleaning or processing when used in soldered or welded assembly. Formed leads are available to facilitate planar mounting of networks on flat circuit boards. Standard lead length is 0.185 inches. Networks can be removed from Mech-Pak carriers with lead lengths up to 0.185 inches.

FORMED LEADS

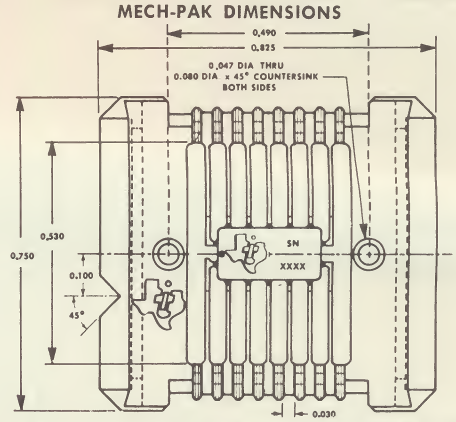


NOTES: a. All dimensions in inches.
b. Not applicable in Mech-Pak Carrier.
c. Measured from center of lead to bottom of package where lead emerges from body.

insulator

An insulator, secured to the back surface of the package, permits mounting networks on circuit boards which have conductors passing beneath the package. The insulator is 0.0025 inches thick and has an insulation resistance of 10 megohms at 25°C.

MECH-PAK DIMENSIONS



NOTES: 1. All dimensions are nominal in inches unless otherwise specified.
2. Overall thickness is 0.175 and nestled height is 0.150 each.

mech-pak carrier

The Mech-Pak carrier facilitates handling the network, and is compatible with automatic equipment used for testing and assembly. The carrier is particularly appropriate for mechanized assembly operations and will withstand temperatures of 125°C for indefinite periods.

ordering instructions

Variations in mechanical configuration of semiconductor networks are identified by suffix numbers shown in a table at the right.

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.185 inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	−6	−7	−1	−2	−3	−4	−5

†Patented by Texas Instruments Incorporated.

‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS 22, TEXAS

PRINTED IN U.S.A.